## REMARKS

Claims 1-45 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the remarks presented herein.

## 35 USC § 101

Claims 1, 17, 18, 23, 33 and 37 are rejected under 35 USC § 101, as allegedly being directed to non-statutory subject matter. The rejection alleges that Claims 1 and 18 fail to recite a "physical transformation." Applicants respectfully traverse. Applicants respectfully assert that Claims 1 and 18 recite, "modifying" an instruction segment, e.g., a pattern of bits, within a computer processor. As is well understood in the art, and as described in the present application, a bit pattern represents physical electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. Hence, bits, bit patterns and "instruction segment(s)" represent physical entities as recited. These physical entities also effect the operation of a processor that executes instruction in order to do useful work, e.g., solve problems, provide output, alter memory contents, etc. Furthermore, Applicants respectfully assert that the recited "modifying" of the recited bit patterns represents a physical transformation.

In the response to arguments section, the rejection alleges "electrical and magnetical [sic] are the natural phenomenon." Applicants traverse. Electrical and magnetic signals as associated with electronic systems, e.g., a computer system, are physical quantities manipulated within a computing machine. Their status within such a computing machine is clearly not a "natural phenomenon," as alleged by the rejection.

In addition, the rejection alleges, "the claim is not useful because no substantial practical application can be found in the claim. Applicants respectfully traverse. Applicants respectfully assert that the present claimed invention is useful, and would be understood as useful to one or ordinary skill in the art Executing instructions on a processor is the foundation of application software and operating system software that supports it. Applicants respectfully assert that such software exists globally and is useful, and is used to direct the operations of a processor, e.g., a microprocessor or central processing unit (CPU) or graphics processing unit (GPU).

In the response to arguments section, the rejection references MPEP §2015. Applicants direct the Examiner to section 2106, "Patentable Subject Matter — Computer-Related Inventions." Applicants respectfully assert that an ability to execute computer instructions, as recited, e.g., by Claim 1, is a useful

result, and is therefore statutory subject matter under 35 USC § 101. Moreover, an ability to modify instructions and execute the modified instructions is clearly statutory subject matter under 35 USC § 101, as indicated by the cited reference Nunomura, which manipulates instructions, albeit in a different manner than disclosed and claimed in the present application.

In the response to arguments section, the rejection alleges that "neither application software nor operating system can be found in the claim." Application software and operating system software were cited as examples of the recited "machine language instruction" to illustrate the utility of embodiments in accordance with the present claimed invention. Applicants stand by the assertion, that embodiment of the present invention have utility by virtue of the software they allow to be executed, e.g., on a computer processor.

For these reasons, Applicants respectfully assert that Claims 1 and 18 fully comply with 35 USC § 101, and that the rejections under 35 USC § 101 are overcome.

Claims 17, 23, 33 and 37 are rejected under similar arguments. Applicants respectfully assert that these Claims overcome the 35 USC § 101 rejections for at least the rationale previously presented.

35 U.S.C. § 102

Claims 1-5, 8, 9-14, 17, 18, 20-23 and 34-36 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Nunomura (US 6,871,274, "Nunomura"). Applicants have carefully reviewed the cited reference and respectfully assert that embodiments of the present invention as recited in Claims 1-5, 8, 9-14, 17, 18, 20-23 and 34-36 are patentable over Nunomura.

With respect to Claim 1, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "fetching a first machine language instruction" as recited by Claim 1. Applicants respectfully assert that the rejection improperly equates the taught "compressed instruction code" with the recited machine language instruction.

In contrast, Nunomura teaches "a compressed instruction code" (column 2, lines 2-3, *inter alia*). In addition, Nunomura teaches that such "compressed instruction code" is accessed by "an instruction code conversion apparatus" (column 2, lines 1-2, *inter alia*) and not by an "instruction decode unit" (column 5 lines 6-20), as are other machine language instructions.

In the response to arguments section, the rejection repeats the above argument and concludes that "therefore, the compress [sic] code was a machine

language instruction." Applicants respectfully assert that the rejection's conclusion does not follow from the cited teachings. Specifically, if the taught instruction decode unit decodes instructions, but does not decode "compressed instruction codes," then the "compressed instruction codes" are not "instructions" as taught by Nunomura.

Further, Nunomura teaches, "an instruction code conversion apparatus converts a first code to a second code longer in bit length than the first code to create an instruction code" (column 2, lines 17-19, *inter alia*). In teaching that an "instruction code" is created, Nunomura teaches that the taught "first code," also known as a "compressed instruction code," is not an "instruction code." Consequently, Applicants respectfully assert that Nunomura teaches that the "compressed instruction code" is not a machine language instruction. Applicants respectfully further assert that one of ordinary skill in the art would not understand the taught "compressed instruction code" to teach or fairly suggest the recited "machine language instruction" as recited by Claim 1.

Still further, Nunomura teaches that the "compressed instruction code" is "unrecognizable as an instruction code." (column 7 lines 30-37).

In the response to arguments section, the rejection appears to ignore the referenced teachings of Nunomura that the "compressed instruction code" is

"unrecognizable as an instruction code" and Applicants' arguments that such teaching shows that the basis for the rejection is improper. Rather, the rejection states that "unrecognizable" is not recited. While the rejection's statement is true, the rejection's argument is not germane because the instant limitation at issue is "machine language instruction" as recited by Claim 1. Nunomura teaches that the "compressed instruction code," which is alleged by the rejection to teach the recited "machine language instruction," is "unrecognizable as an instruction code." Applicants assert that something that is "unrecognizable as an instruction code" is not the recited "machine language instruction" as recited by Claim 1.

For these reasons, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 1, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "modifying said instruction segment to form a second machine language instruction" as recited by Claim 1.

Claim 1 recites that the instruction segment is part of a first machine language instruction. Even if, *arguendo*, the taught "compressed instruction code" suggests a machine language instruction, Nunomura fails to teach or

fairly suggest the limitation of "modifying said instruction segment" as recited by Claim 1.

As taught by Nunomura, a segment of the "compressed instruction code" is replaced by a second code "longer in bit length than the first code" (column 2 lines 18-19). For example, Figure 4 shows a four-bit "index" mapping into a 24 bit op code. Applicants respectfully assert that a code segment "longer in bit length than the first code" as taught by Nunomura, cannot be the recited "instruction segment" that is part of the recited first machine language instruction. Applicants respectfully assert that an "instruction segment" as recited by Claim 1 cannot simultaneously be both four bits and 24 bits long. Further, Applicants respectfully assert that an alleged first machine language instruction taught as 16 bits in length cannot comprise an "instruction segment" of 24 bits in length.

In the response to arguments section, the rejection ignores the argument presented. Rather, the rejection states that "claim 1 never recites that the instruction segment cannot be both four and 24 bits long." While the rejection's statement is true, the rejection's argument is not germane because the instant limitation at issue is an "instruction segment" as recited by Claim 1. The rejection equates a four bit field and a 24 bit field as both being the recited segment. While both a four bit field or a 24 bit field may be segments of an

instruction field, they cannot be the same segment. Applicants assert that 4 is not equal to 24, and that a field taught as 4 bits cannot also be a 24 bit field, as alleged by the rejection.

Further, the alleged 24-bit instruction segment will not fit in the 12 or 16-bit machine language instructions taught by Nunomura. Thus, the 24-bit field cannot be a segment of a 12 or 16 bit machine language instruction.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 8, 17, 33 and 37 are rejected under the same rationale as applied to Claim 1. Applicants respectfully assert that Claims 8, 17, 33 and 37 overcome the rejections of record for at least the rationale previously presented with respect to Claim 1, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 2-7, 9-16, 18-22, 34-36 and 38-45 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 2, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "substitut(ing) a bit pattern of a subset of said instruction segment" as recited by Claim 2. In contrast, Nunomura teaches "substituting" more bits than an instruction segment contains. In this manner, Nunomura actually teaches away from the recited limitation of substituting a subset of bits of an instruction segment, as recited by Claim 2.

In the response to arguments section, the rejection concedes that Nunomura teaches "substituting" more bits than an instruction segment contains. Applicants assert that a subset cannot contain more elements than the set, by definition. Consequently, the recited "subset" can be no larger than the recited instruction segment. As Nunomura teaches substituting more bits than an instruction segment contains, the substituted bits cannot be a subset, or even the instruction segment itself, as they are too small. The rejection attempts to place too many bits, as taught by Nunomura, into too small a bit field, as recited.

For this additional reason, Applicants respectfully assert that Claim 2 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 4, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "executing microcode" as recited by Claim 4. Applicants respectfully assert that Nunomura is silent as to such recited microcode. Applicants respectfully note that Figure 4, cited in rejecting Claim 4, refers to compressed instructions and instruction codes. Such codes do not teach or fairly suggest microcode, as used in the art, as explained in the present application and as recited in the instant claim.

In the response to arguments section, the rejection persists in improperly equating "compressed instructions" and "instruction codes" with the recited "microcode." The term "microcode" is well known to those of ordinary skill in the art and further explained in the present application. Applicants assert that the term "microcode" is used consistent with its ordinary meaning. In addition, "an applicant is entitled to be his or her own lexicographer." *In re Paulsen*, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994).

For this additional reason, Applicants respectfully assert that Claim 4 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 10, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "advancing a queue structure to a next entry storing instruction modification information in said memory" as recited by Claim 10. Applicants respectfully assert that Nunomura is completely silent as to such queue structures. Applicants respectfully note that Figure 2, cited in rejecting Claim 10, refers to a table mapping an index code to a non-compressed instruction code. Such a table does not teach or fairly suggest a queue, as used in the art, as explained in the present application and as recited in the instant claim.

In the response to arguments section, the rejection makes clear that it ignores the plain meaning of the term "queue." As is know to those of ordinary skill in the data processing arts, a "queue" is a first in, first out data structure. In contrast, the rejection states, "any queue contains entries in general." Thus the rejection improperly equates a queue with any data structure. Under the rejection's improper equivalence, this response may be considered a queue. Applicants traverse, and reiterate that the rejection's equivalence is improper and that Nunomura fails to teach or fairly suggest the instant limitation.

For this additional reason, Applicants respectfully assert that Claim 10 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 11, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "advancing a pointer to indicate said next entry storing instruction modification information in said (queue)" as recited by Claim 11. Applicants respectfully assert that Nunomura is completely silent as to such queue structures or queue pointers. Applicants respectfully note that Figure 2, cited in rejecting Claim 11, refers to a table mapping an index code to a non-compressed instruction code. Such a table does not teach or fairly suggest a queue or queue pointer or advancing a queue pointer, as used in the art, as explained in the present application and as recited in the instant claim.

For this additional reason, Applicants respectfully assert that Claim 11 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 34, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "decoding said trigger pattern to identify said portion of said machine language instruction" as recited by Claim 34. Applicants respectfully assert that Nunomura is completely silent as to a trigger pattern identifying a portion of a machine language instruction. Applicants respectfully note that Figure 2, cited in rejecting Claim 34, refers to

a table mapping an index code to a non-compressed instruction code. Such a table does not teach or fairly suggest identifying a portion of an instruction for modification, as used in the art, as explained in the present application and as recited in the instant claim.

In contrast, Nunomura teaches that the same portion of a compressed instruction code, e.g., the index in Figure 4, is always the portion changed. Hence, there is no need in Nunomura to decode anything in order to determine which portion of a compressed instruction code is to be substituted, and therefore Nunomura fails to teach or fairly suggest "decoding said trigger pattern to identify said portion of said machine language instruction" as recited by Claim 34.

In the response to arguments section, the rejection alleges that the taught table identifies a portion of an instruction for modification. Applicants traverse. While the table may include information that is inserted into an instruction, the table does not identify what portion of an instruction is modified.

For this additional reason, Applicants respectfully assert that Claim 34 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

35 U.S.C. § 103

Claims 6, 7, 16, 23-27, 32, 38 and 39 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Nunomura (US 6,871,274, "Nunomura") in view of Rim (US 6,202,143, "Rim"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claims 6, 7, 16, 23-27, 32, 38 and 39 are patentable over Nunomura in view of Rim.

With respect to Claims 6, 7, 16, 23-27, 32, 38 and 39, Applicants respectfully assert that the proposed manner of combination of Nunomura in view of Rim is not supported by the references. Rim teaches multiple program memories for storing multiple sizes of instruction words, and that the multiple program memories "preferably have different (bus) widths" (Abstract). In contrast, Nunomura teaches a single memory with a single bus size. Applicants respectfully assert that one of ordinary skill in the art would not be motivated to combine these references in the manner suggested because of the complexity of Rim in contrast to the relative simplicity of Nunomura.

In the response to arguments section, the rejection states that "applicat failed to explain why the complexity of Rim in contrast to the relative simplicity

of Nunomura would not have combined the references." Applicants respectfully assert that one of ordinary skill in the art would understand a simpler system to be preferable to a more complex system, for accomplishing the same result. For example, "increased complexity" is not an advantage, and therefore provides no rationale for combining references, particularly in the manner proposed by the rejection. In addition, the "Examiner would like to point out the complexity of Rim in addition to the relative simplicity of Nunomura would have motivated one of ordinary skill in the art to combine the references." Herein, the rejection puts forth the proposition that it is inherently desirable to combine complex systems with simple systems. Applicants traverse, and note that no art is introduced to support the rejection's proposition.

For this reason, Applicants respectfully assert that the proposed combination of Nunomura in view of Rim does not motivate the claimed subject matter, and that all rejections dependent upon this combination of references are overcome. The rejection proposes, as motivation for the proposed manner of combination, that one of ordinary skill would be motivated to increase the adaptability of Nunomura to accept long instruction words. Applicants respectfully traverse. There is no teaching in the prior art as to the desirability of modifying Nunomura to accept VLIW instructions. Moreover, Nunomura fails to teach or fairly suggest the multiple instruction units necessary to process a VLIW instruction. Thus, even if Nunomura was modified in view of

Rim to "recognize() ... specific instruction type with corresponding width of the Rim's VLIW," the proposed combination would be unable to execute such VLIW instructions. Applicants respectfully assert that one of ordinary skill in the art would not be motivated to modify Nunomura in view of Rim, in the manner proposed by the rejection, to "recognize" VLIW instructions in spite of a lack of capability to execute such instructions.

In the response to arguments section, the rejection alleges, "one of ordinary skill in the art should be able to recognize the use of VLIW in general." While one of ordinary skill in the art may be able to recognize the use of VLIW, there is no suggestion in the art to motivate use of VLIW. Moreover, the cited references are unable to execute VLIW instructions. Herein, particularly in its use of the term "recognize," the rejection demonstrates its use of impermissible hindsight to craft a combination of cited and uncited references guided only by Applicants disclosure and claims.

For this additional reason, Applicants respectfully assert that the proposed manner of combination of Nunomura in view of Rim is is not suggested by the cited references, and that all rejections dependent upon this combination of references are overcome. Applicants respectfully solicit allowance of Claims 6, 7, 16, 23-27, 32, 38 and 39.

Further, Nunomura teaches a method of storing instructions in a compressed format. In contrast, Rim teaches a method of expanding a complete uncompressed instruction with meaningless filler (a "NOP" or no operation instruction) to fill a wide bus. Applicants respectfully assert that, in consideration of the whole of the teachings of Nunomura and Rim, one of ordinary skill in the art would not be motivated to modify a decompression process with a process that places meaningless filler into an instruction word. Moreover, Nunomura has no need for the filler methods of Rim, as Nunomura has a single bus and a single bus width.

In the response to arguments section, the rejection fails to understand the phrase "stuff meaningless filler." While Applicants assert that the plain meaning of this phrase is clear to those of ordinary skill in the art, the following additional comments are offered. Rim teaches "short" instructions, e.g., instructions that are less wide than a data bus. To fill up the bus, Rim teaches addition of meaningless data, e.g., a NOP instruction. Nunomura has no need for being filled with the filler bits taught by Rim.

For this further reason, Applicants respectfully assert that the proposed combination of Nunomura in view of Rim is improper, and that all rejections dependent upon this combination of references are overcome. Applicants respectfully solicit allowance of Claims 6, 7, 16, 23-27, 32, 38 and 39.

With respect to Claims 6, 7, 16, 23-27, 32, 38 and 39, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "fetching a first machine language instruction" as recited by the instant Claims, for at least the rationale previously presented with respect to Claim 1. As Rim fails to correct this deficiency of Nunomura, Applicants respectfully assert that Claims 6, 7, 16, 23-27, 32, 38 and 39 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 2-7, 9-16, 34-36 and 38-45 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 6, Applicants respectfully assert that Nunomura in view of Rim fails to teach or fairly suggest the limitation of "wherein said first machine language instruction comprises a very long instruction word" as recited by Claim 6. Applicants are unclear as to what format a compressed instruction code might have under the modification proposed by the rejection, but respectfully assert that such a compressed instruction code would not be a very long instruction word as specifically recited by Claim 6.

While Nunomura in view of Rim may allegedly teach some form of manipulating a first bit pattern to produce a second bit pattern, wherein the second bit pattern is a VLIW instruction, the recited limitation refers to accessing a VLIW instruction, e.g., the allegedly taught first bit pattern must be a VLIW instruction. Applicants understand that it is the intention of Nunomura is to reduce the size of such compressed instruction codes. Hence, Nunomura teaches away from the recited fetching VLIW machine language instructions as recited by Claim 6..

In the response to arguments section, the rejection alleges, "Nunomura's intention is to minimize the length of compressed instruction codes. Therefore, Nunomura suggested the need for reducing the VLIW." While, *arguendo*, Nunomura may teach minimizing the length of compressed instruction codes, Claim 6 recites "fetching" a very long instruction word machine language instruction. The rejection alleges a teaching of accessing a compressed very long instruction word that is "unrecognizable as an instruction code." (column 7 lines 30-37). Consequently, what is taught as accessed by Nunomura is not an instruction and therefore not a VLIW. Accessing something that is not an instruction fails to teach the claimed limitation of "fetching" an instruction.

For this additional reason, Applicants respectfully assert that Claim 6 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 23, Applicants respectfully assert that Nunomura in view of Rim fails to teach or fairly suggest modifying a "very long instruction word" as recited by Claim 23. As described previously with respect to Claim 6, Nunomura in view of Rim may allegedly teach some form of manipulating a first bit pattern to produce a VLIW instruction. However, Applicants respectfully assert that the first bit pattern taught by Nunomura in view of Rim is not a VLIW instruction, as recited by Claim 23.

For this additional reason, Applicants respectfully assert that Claim 23 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 24-32 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

Claims 28-31, 40-44 and 45 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Nunomura (US 6,871,274, "Nunomura") in

view of Rim (US 6,202,143, "Rim") and further in view of Ebicioglu et al (US 6,112,299, "Ebicioglu"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claims 28-31, 40-44 and 45 are patentable over Nunomura in view of Rim and further in view of Ebicioglu.

For at least the rationale previously presented with respect to Claims 6, 7, 16, 23-27, 32, 38 and 39, Applicants respectfully assert that the proposed combination of Nunomura in view of Rim is improper, and that all rejections dependent upon this combination of references are overcome. For this reason, Applicants respectfully assert that Claims 28-31, 40-44 and 45 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 28-31, 40-44 and 45 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

With respect to Claim 28, Applicants respectfully assert that Nunomura in view of Rim fails to teach or fairly suggest the limitation of said trigger pattern identifies an arithmetic logic unit segment" as recited by Claim 28. As recited by Claim 23, from which Claim 28 depends, the recited "trigger pattern initiate(s) modification of a segment of said very long instruction word."

While Ebicioglu may imply that various portions of a VLIW may be identified, Ebicioglu further teaches, "each parcel 510 occupies specific bit positions and controls those hardware units hard-wired to those positions" (column 11 lines 15-36). By teaching hardware units hard-wired to specific bit positions, Ebicioglu teaches away from embodiments of the present invention that recite a "trigger pattern identifies an arithmetic logic unit segment" as recited by Claim 28.

In the response to arguments section, the rejection appears to take Claim 28 out of context, e.g., the rejection ignores the limitations of the base Claim. The rejection asserts that Ebicioglu, in combination with additional uncited knowledge, teaches identification of the recited arithmetic logic unit segment. Applicants respectfully assert that Ebicioglu's teaching of hardware units being "hard-wired," precludes modification of such bits. For example, as bits are loaded into Ebicioglu, they begin their "hard-wired" function. There is no teaching to support changing such bits. Consequently, the proposed modification, to modify Ebicioglu's "hard-wired" bits, is not taught or fairly suggested by the cited art. Moreover, Applicants respectfully assert that one of ordinary skill in the art would have no expectation of success for the rejection's proposed modification.

In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991), there must be a reasonable expectation of success, and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. Applicants reiterate that there is no expectation of success, reasonable or otherwise, for the rejection's proposed modification, and that the rejection employs impermissible hindsight to craft a combination of cited and uncited references guided only by Applicants disclosure and claims.

For this additional reason, Applicants respectfully assert that Claim 28 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

## CONCLUSION

Claims 1-45 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the amendments and remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

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Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060